PCSA

DEPCA Hardware Reference Manual

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The Reader's Comments form at the end of this document requests the user's critical evaluation to assist us in preparing future documentation.

FCC NOTICE: The equipment described in this manual generates, uses, and may emit radio frequency energy. The equipment has been type tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such radio frequency interference when operated in a commercial environment. Operation of this equipment in a residential area may cause interference, in which case the user at his own expense may be required to take measures to correct the interference.

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About This Manual

The Personal Computing Systems Architecture (PCSA) is an extension of the DIGITAL systems and networking architecture that merges VMS and MS-DOS environments. The PCSA network can include VAX or MicroVAX servers running VAX/VMS Services for MS-DOS. The PCSA network also includes the DECnet/PCSA Client software that runs on PC and VAXmate workstations. Other PCSA products include the ThinWire Ethernet products and other peripherals, such as the LN03 Plus and the LA75 Companion printers.

The DIGITAL PCSA network fully integrates all the elements of personal and corporate computing required for direct information access and sharing. Thus, it has computing and communication capabilities substantially better than those of conventional PC local area networks (LANs).

Manual Objectives

This manual provides information required to program the DIGITAL Ethernet personal computer adapter (DEPCA) at the hardware level. However, the recommended programming interface is the data-link layer (firmware), which is described in the *Data Link Programmer's Reference Manual*.

Vendor-specific network applications can be easily written using the data-link firmware interface provided with the DEPCA. There are no meaningful performance advantages to be gained by programming the hardware directly. Good network software design dictates a modular, layered approach based on the ISO 7-layer model. The data link is the lowest hardware-independent level. All other network software should use the data-link layer to communicate with the hardware.

Additionally, there are subtle differences among different revisions of the local area network controller for Ethernet (LANCE) chip used on the DEPCA. The data link takes these differences into account, but this manual does not provide that level of detail.

Intended Readers

This manual is intended for programmers who want to program the DEPCA at the hardware level. This manual is not a tutorial. It assumes that the reader has a working knowledge of networking concepts and programming at the hardware level.

Manual Organization

This manual consists of three chapters and an index.

Chapter 1	Contains an introduction to the DEPCA hardware.
Chapter 2	Describes the network interface.
Chapter 3	Describes the mouse interface.

1
Introduction to the DEPCA

The DIGITAL Ethernet personal computer adapter (DEPCA) provides the hardware and firmware components for an Ethernet network interface and a mouse interface.

NOTE
This manual provides information required to program the DEPCA at the hardware level. However, the recommended programming interface is the data-link layer (firmware), which is described in the *Data Link Programmer's Reference Manual.*

The DEPCA is a full-length card that fits in an 8-bit or 16-bit bus connector. Thus, the DEPCA can be installed in an IBM Personal Computer, IBM Personal Computer XT, IBM Personal Computer AT, and compatibles.

Network Interface External Connector

The DEPCA connects to the network coaxial cable through a BNC-type T-connector. The DEPCA complies with IEEE 802.3 10BASE2 specifications. The cable shield is isolated from the workstation logic and chassis ground. If local electrical codes require grounding, the cable shield must be externally grounded by the interconnect equipment. The DEPCA does not contain a 50-ohm line terminator. The 50-ohm line terminator must be supplied externally, as required by the connection topology.

A DB-15S connector is available as an optional attachment unit interface (AUI) network interface.

Mouse Interface External Connector

The mouse connector is a 7-pin circular connector.

DEPCA Buffer RAM and ROM

The DEPCA provides 48 Kbytes of dual-port static RAM and 16 Kbytes of ROM (64 Kbytes total). For certain systems and option card configurations where RAM and/or option ROM address space is at a premium, the DEPCA provides a reduced buffer mode that provides 16 Kbytes of dual-port static RAM and 16 Kbytes of ROM (32 Kbytes total).

The system bus accesses the buffer RAM as 8-bit bytes. CPU instructions that contain 16-bit word memory references result in two back-to-back 8-bit byte access cycles. The method of conversion between a 16-bit word and two 8-bit bytes depends on the system in which the DEPCA is installed. In all cases, the conversion is accomplished by the microprocessor or system bus converter logic, not by the DEPCA. Because the DEPCA does not do the conversion, you should avoid instructions that contain word memory references. The two back-to-back 8-bit byte access cycles are not interruptable by direct memory access (DMA) requests. Because system bus access to the buffer must be arbitrated on a cycle-by-cycle basis, the two back-to-back access cycles can incur excessive wait states and degrade system bus DMA latency to unacceptable levels.

DEPCA Jumper Configurations

The DEPCA provides jumpers for selecting:

- Input/output (I/O) address ranges
- Memory address ranges
- Interrupt vector assignments
- Remote boot

The remaining sections of this chapter describe the various jumper configurations that are of interest to the programmer. For complete jumper location and installation information, refer to the *DEPCA Owner's Manual*.

I/O Address Range Selection

Jumper location W6 selects between two I/O address ranges. When jumper W6 is installed, the primary I/O address range (0300H - 030FH) is selected. When jumper W6 is removed, the secondary I/O address range (0200H - 020FH) is selected.

All registers are located within the selected I/O address range. It is not possible to select the primary I/O address range for some registers and the secondary I/O address range for other registers.

The default selection is the primary I/O address range.

Memory Base Address and Size Selection (for Rev E and higher)

The combination of jumper locations W7 and W8 select the base address of the RAM buffer and the ROM firmware and the size of the RAM buffer. Table 1–1 describes the possible jumper combinations. In the table, the terms IN and OUT refer to the state of the indicated jumper. IN means installed and OUT means removed.

The default selections are the primary address range and 64 Kbyte mode.

Table 1–1 DEPCA Memory Address and Size Selection

W7	W8	RAM Addresses	ROM Addresses	Description
IN	IN	D0000H-DBFFFH	DC000H-DFFFFH	Primary 64 Kbyte
IN	OUT	D8000H-DBFFFH	DC000H-DFFFFH	Primary 32 Kbyte
OUT	IN	E0000H-EBFFFH	EC000H-EFFFFH	Secondary 64 Kbyte
OUT	OUT	C8000H-CBFFFH	CC000H-CFFFFH	Secondary 32 Kbyte

Interrupt Vector Selections

The DEPCA provides five jumpers, W1 through W5, that select the interrupt request (IRQ) lines used by the network interface and the mouse interface. Each jumper location has three pins. When the jumper is installed on the top two pins, that jumper location selects the mouse IRQ line. When the jumper is installed on the bottom two pins, that jumper location selects the network interface IRQ line. When no jumper is installed at a jumper location, that IRQ line is not used by the DEPCA. Table 1–2 lists the possible jumper selections for the mouse and network interface IRQ lines. In the table, the terms TOP and BOT refer to a jumper installed in the top (TOP) or bottom (BOT) locations.

The default selection is IRQ3 for the network interface and IRQ2 for the mouse.

Table 1–2 DEPCA IRQ Selections

Jumper	IRQ	Installed	Description
W1	2	TOP	Mouse interface
		BOT	Network interface
W2	3	TOP	Mouse interface
		BOT	Network interface
W3	4	TOP	Mouse interface
		BOT	Network interface
W4	5	TOP	Mouse interface
		BOT	Network interface
W5	7	TOP	Mouse interface
		BOT	Network interface

Remote Boot Selection

Jumper location W16 enables and disables the remote network boot feature of the DEPCA firmware (see the *Data Link Programmer's Reference Manual*). When jumper W16 is installed, remote network boot is disabled. When jumper W16 is removed, remote network boot is enabled.

Successful operation of the remote network boot feature requires network server software that supports remote network boot.

2

Network Interface Hardware

Digital Equipment Corporation recommends that you avoid programming the hardware interface directly. Instead, programmers should use the MS-NET session level interface, DECnet-DOS session level interface, and the data-link interface to access the network. For additional information about these software interfaces, see *Data Link Programmer's Reference Manual* or the *DECnet-DOS Programmer's Reference Manual.*

The remainder of this chapter discusses the following topics:

- Functional description of the network interface hardware
- Programming sequence
- Register descriptions
- Physical description
- Physical address field
- Logical address filter field
- Buffer management
- Receive descriptor rings
- Transmit descriptor rings

Functional Description of the Network Interface Hardware

The network interface (NI) consists of three main integrated circuits. The hardware also includes a small number of discrete components, system bus interfacing devices, and a female BNC connector mounted directly on DEPCA printed circuit board. The BNC connector connects the NI to the network. The three integrated circuits in the NI are the:

- Coax transceiver interface (CTI)
- Serial interface adapter (SIA)
- Local area network controller for Ethernet (LANCE)

The Coax Transceiver Interface (CTI)

The CTI interfaces to the coaxial cable by a BNC connector. The CTI performs transmit, receive, and collision detection functions for the network controller. The CTI is electrically isolated from the other devices as required by IEEE 802.3 specifications.

The Serial Interface Adapter (SIA)

The SIA interfaces to the CTI through an isolation transformer. The SIA performs Manchester phase encoding and decoding of the data transferred over the network. The SIA also interfaces with the LANCE. The SIA filters noise and interprets collisions for the LANCE circuit.

The Local Area Network Controller for Ethernet (LANCE)

The LANCE converts data between the network serial format and the system byte-wide format. The LANCE is the primary interface between the network hardware and the rest of the workstation.

Additional information about the LANCE can be found in the Advanced Micro Devices document *MOS Microprocessors and Peripherals 1985 Data Book*.

In receive mode, the LANCE:

1. Receives information from the SIA.
2. Converts the serial network bit stream into a parallel (8-bit wide) byte stream.
3. Strips the Ethernet preamble and synchronization pattern.
4. Checks and removes the CRC bits.
5. Uses direct memory access and a 24-bit-wide physical address to place the information in dual-port buffer memory located in the CPU address space.

In transmit mode, the LANCE:

1. Uses DMA to read data from the dual-port buffer memory.
2. Converts the data to a serial bit stream.
3. Adds a preamble and synchronizing pattern.
4. Calculates and adds the CRC at the end of the data packet.
5. Passes the data packet to the SIA for transmission on the ThinWire Ethernet.

Programming the LANCE

This section defines the control registers, status registers, and the data structures that are used to program the hardware interface.

The LANCE is controlled by a set of four control and status registers (CSRs) and three data structures. The CSRs are accessible within the CPU I/O address space and the data structures located in the CPU memory address space. After the LANCE is enabled, it acquires additional operating parameters by accessing the data structures. The LANCE accesses dual-port buffer memory through bus arbitration between the LANCE and the CPU.

After the LANCE is programmed, it independently manages the data structures and transfers data packets on the ThinWire Ethernet.

The three data structures accessed by the LANCE are:

- Initialization Block
- Receive and Transmit Descriptor Rings
- Data Buffers

Initialization Block

The initialization block consists of 12 contiguous words of memory starting on a word boundary. The controlling program stores the operating parameters in the initialization block. To acquire the operating parameters, which are necessary for device operation, the LANCE reads the initialization block. The initialization block contains the:

- Mode of operation
- Physical address
- Logical address mask
- Location of receive and transmit descriptor rings
- Number of entries in receive and transmit descriptor rings

Receive and Transmit Descriptor Rings

The receive and transmit descriptor rings are two ring structures: one for incoming and the other for outgoing packets. Each entry in the rings is four words, and must start on a quadword boundary. The descriptor rings contain the buffer address, length, and status.

Data Buffers

Data buffers are contiguous portions of memory reserved for buffering packets. Data buffers can begin on arbitrary byte boundaries. Entries in the Receive and Transmit Descriptor Rings point to the data buffers.

Programming Sequence

The general programming sequence of the LANCE is:

1. Load CSR1 and CSR2, which identifies the location of an initialization block in memory.
2. Load CSR3, which sets the operating mode of the LANCE.
3. Set the INIT and STRT bits in CSR0, which causes the LANCE to load the information from the initialization block and to access the descriptor rings.

   NOTE

   Some versions of the LANCE require the initialization procedure to set the INIT bit, wait for IDON, and then set the START bit.

NOTE
The ThinWire Ethernet interface conforms to the IEEE 802.3 specification, which requires a frequency accuracy of ±0.01%. The crystal oscillator in the DEPCA network hardware requires 1 Ms after poweron to achieve ±10% accuracy, and 10 seconds to achieve ±0.01% accuracy. Therefore, the network interface is considered operational 10 seconds after power is applied to the DEPCA.

On powerup, the workstation diagnostics ensure the required 10-second settling time.

Register Description

The network interface uses three physical I/O ports as registers: two in the LANCE, and one in the interface logic. The registers in the LANCE comprise five logical registers, for a total of six logical registers in the Network Interface (NI).

The LANCE internal control and status registers (CSRs) are accessed through its two bus-addressable ports, a register address port (RAP), and a register data port (RDP). The internal CSRs are read (or written) in a two-step operation. The address of the CSR is written into the RAP. Then the data is read from (or written into) the selected CSR through the RDP. Once written, the address in RAP remains unchanged until rewritten.

NOTE
The 16-bit LANCE registers must be accessed using word I/O instructions. Using byte I/O instructions can provide unpredictable results.

Table 2–1 describes the registers and their addresses.

Table 2–1 Network Interface Registers

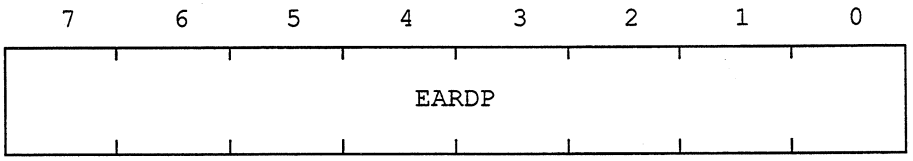
Primary I/O Address	Secondary I/O Address	R/W	Register Width	Description
0300H	0200H	R/W	8-bit	Network Interface Control/Status (NI CSR)
0304H	0204H	R/W	16-bit	LANCE Register Data Port (RDP)
0306H	0206H	R/W	16-bit	LANCE Register Address Port (RAP) 0 = Control/Status Register 0 (CSR0) 1 = Control/Status Register 1 (CSR1) 2 = Control/Status Register 2 (CSR2) 3 = Control/Status Register 3 (CSR3)
030CH	020CH	R	8-bit	Ethernet Address-ROM Data Port (EARDP)

Network Interface Control/Status Register (NI CSR)

7	6	5	4	3	2	1	0
RES	RES	BUF	RBE	AAC	IM	IEN	LED

Bit	R/W	Description
7-6		RES — Reserved (undefined)
5	R	BUF — Network buffer memory size jumper-select status 0 = 48 Kbytes (always 0 on revision D or lower) 1 = 16 Kbytes
4	R	RBE — Remote boot enable jumper-select status 0 = Disabled 1 = Enabled
3	R/W	AAC — Address-ROM address counter control 0 = Reset to zero (power-on default) 1 = Count To reset the address-ROM address counter, set the ACC bit to zero, perform a "dummy" read of the address-ROM data port (to clock in the reset command), then set the AAC bit to one.
2	R/W	IM — Interrupt mask (for LANCE interrupt only) 0 = Interrrupt line active (power-on default) 1 = Interrupt line forced inactive
1	R/W	IEN — Interrupt line tri-state enable control 0 = Tri-state (power-on default) 1 = Enabled
0	R/W	LED — LED diagnostic indicator control 0 = LED OFF 1 = LED ON

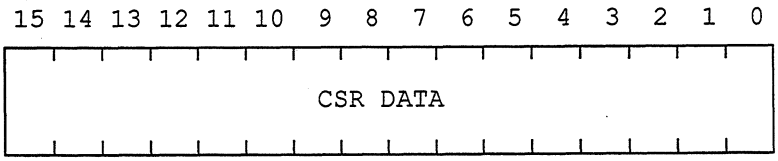
Ethernet Address-ROM Data Port (EARDP)



Bit	R/W	Description
7-0	R	EARDP — Ethernet address-ROM data port The EARDP is a read-only port. The actual ROM address that is read is controlled by the Ethernet address-ROM address counter (EARAC). Each time the EARDP is read, the EARAC increments to the next ROM location. After 32 read accesses of the EARDP, the EARAC wraps to zero. The EARAC is cleared at power-on, system reset, or by the ACC bit in the NI CSR. To reset the EARAC, set the NI CSR ACC bit (bit 3) to zero, perform a "dummy" read of the EARDP (to clock in the reset command), then set the NI CSR AAC bit (bit 3) to one.

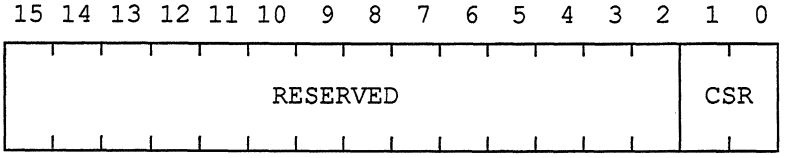
The DEPCA has a 32-byte ROM, which contains the hardware Ethernet node address. This is the standard Ethernet address PROM.

Register Data Port (RDP)



Bit	R/W	Description
15-0	R/W	CSR DATA Writing data into RDP writes the data into the CSR selected in RAP. Reading the data from RDP reads the data from the CSR selected in RAP. CSR1, CSR2, and CSR3 are accessible only when the STOP bit (CSR0) is set. If the STOP bit (CSR0) is not set while attempting to access CSR1, CSR2, or CSR3, the LANCE returns READY, but a read operation returns undefined data and a write operation is ignored.

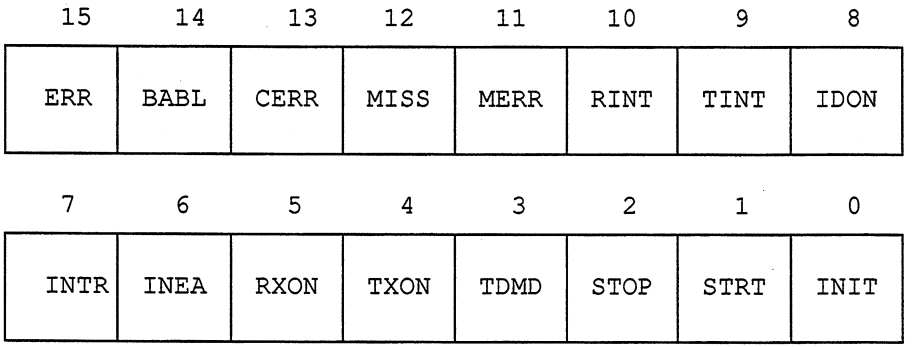
Register Address Port (RAP)



Bit	R/W	Description
15-2		Reserved (Always 0)
1-0	R/W	CSR — Control/status register select 0 = CSR0 accessed through RDP 1 = CSR1 accessed through RDP 2 = CSR2 accessed through RDP 3 = CSR3 accessed through RDP

The register address port is cleared by STOP or bus RESET.

Control and Status Register 0 (RAP = 0)



Bit	R/W	Description
15	R	ERR — Error 0 = The four bits BABL, CERR, MISS and MERR are all equal to 0. 1 = One or more of the four bits, BABL, CERR, MISS, or MERR are equal to 1.
14		BABL — Babble
	R	0 = Less than 1519 bytes of data were transmitted. 1 = 1519 bytes of data, or more, were transmitted. BABL indicates a transmitter error, caused by the transmitter being on longer than the time required to send the maximum length packet. The LANCE transmits data until the transmit buffer byte count equals zero. The LANCE assumes the Ethernet transmission is limited by the physical channel interface. If INEA equals 1, an interrupt is generated when BABL is set.
	W	0 = No effect 1 = Clears this bit (BABL) BABL is read/clear only. BABL is cleared by bus RESET or setting the STOP bit (CSR0).

Bit	R/W	Description
13		CERR — Collision error
	R	0 = No collision error 1 = Collision error The collision input failed to activate within 2 µs after a transmission, started by the controller, was completed. Collision after transmission is a test feature of the transceiver.
	W	0 = No effect 1 = Clears this bit CERR is read/clear only. CERR is cleared by bus RESET or setting the STOP bit (CSR0).
12		MISS — Missed packet
	R	0 = Receiver owns a receive buffer or the silo has not overflowed 1 = The receiver lost a packet because it did not own a receive buffer and the silo has overflowed, indicating loss of data. silo overflow is not reported because there is no receive ring entry in which to write the status.
	W	0 = No effect 1 = Clears this bit If INEA equals 1 and MISS equals 1, an interrupt is generated. MISS is read/clear only. MISS is cleared by bus RESET or setting the STOP bit (CSR0).
11		MERR — Memory error
	R	0 = No memory error 1 = LANCE is the bus master and has not received READY within 25.6 µs after asserting the address on the DAL lines. When a memory error is detected, the receiver and transmitter are turned off. If INEA equals 1, an interrupt is generated.
	W	0 = No effect 1 = Clears this bit MERR is read/clear only. MERR is cleared by bus RESET or setting the STOP bit (CSR0).

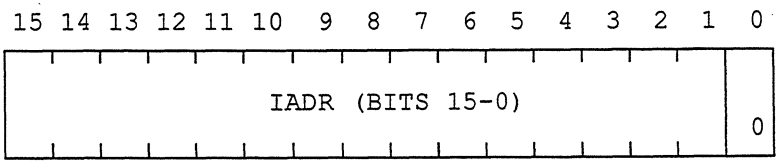
Bit	R/W	Description
10		RINT — Receiver interrupt
	R	0 = No receiver interrupt
		1 = Receiver interrupt
	W	0 = No effect
		1 = Clears this bit
		When the status for an entry in the receive descriptor ring is updated, RINT is set to 1.
		If INEA equals 1, when RINT is set, an interrupt is generated.
		RINT is read/clear only. RINT is cleared by bus RESET or setting the STOP bit (CSR0).
9		TINT — Transmitter interrupt
	R	0 = No transmitter interrupt
		1 = When the status for an entry in the transmit descriptor ring is updated.
	W	0 = No effect
		1 = Clears this bit
		If INEA equals 1 when TINT is set, an interrupt is generated.
		TINT is read/clear only. TINT is cleared by bus RESET or setting the STOP bit (CSR0).
8		IDON — Initialization done
	R	0 = Initialization procedure not completed
		1 = LANCE has completed the initialization procedure started by setting the INIT bit. When IDON is set, the LANCE has read the initialization block from memory and stored the new parameters.
		If INEA equals 1 when IDON is set, an interrupt is generated.
	W	0 = No effect
		1 = Clears this bit
		IDON is read/clear only. IDON is cleared by bus RESET or setting the STOP bit (CSR0).

Bit	R/W	Description
7	R	INTR — Interrupt flag 0 = BABL, MISS, MERR, RINT, TINT, and IDON are all equal to 0 1 = One or more of the following interrupt-causing conditions has occurred: BABL, MISS, MERR, RINT, TINT, IDON. If INEA equals 1 and INTR equals 1, the INTR L I/O pin will be low. INTR is cleared by bus RESET or setting the STOP bit (CSR0). INTR is also cleared by clearing the conditions that caused the interrupt.
6	R/W	INEA — Interrupt enable 0 = The INTR L I/O pin will be high, regardless of the state of INTR. 1 = If INTR equals 1, the INTR L I/O pin will be low. When the interrupt flag is set, INEA allows the INTR L I/O pin to be driven low. If INEA equals 1, INEA is cleared by bus RESET or setting the STOP bit (CSR0).
5	R	RXON — Receiver ON 0 = Receiver disabled 1 = Receiver enabled If IDON equals 1 and the mode field DRX equals 1 or a memory error (MERR = 1) has occurred, RXON equals 0. If IDON equals 1, STRT is set in CSR0, and DRX equals 0 in the mode field, then RXON equals 1. RXON is cleared by bus RESET or setting the STOP bit (CSR0).
4	R	TXON — Transmitter On 0 = Transmitter enabled 1 = Transmitter disabled If IDON equals 1 and the mode field DTX equals 1 or an underflow, retry, or memory (MERR) error has occurred, TXON equals 0. If INIT equals 1, STRT equals 1, and the mode field DTX equals 0, TXON equals 1. TXON is cleared by bus RESET or setting the STOP bit (CSR0).

Bit	R/W	Description
3		TDMD — Transmit demand
	R	0 = The packet is sent subject to the 1.6-millisecond polling interval delay.
		1 = The packet is transmitted without the typical delay of the 1.6 millisecond polling interval.
	W	0 = No effect
		1 = Clears this bit
		TDMD, when set, causes the LANCE to access the transmit descriptor ring without waiting for the poll time interval to elapse. TDMD need not be set to transmit a packet; it merely hastens the LANCE response to a transmit descriptor ring entry insertion by the software.
		TDMD is cleared by bus RESET or setting the STOP bit (CSR0). TDMD is cleared by the LANCE after the transmit descriptor ring is accessed.
2	R/W	STOP
		0 = No effect
		1 = Disables LANCE from all external activity and clears internal logic
		STOP set is the equivalent of asserting bus RESET L. Stop will terminate all LANCE activities asynchronously. The LANCE remains inactive and STOP remains set until the STRT or INIT bit is set.
		If STRT, INIT, and STOP are all set together, STOP will override the other bits and only STOP will be set.
		STOP is cleared by setting INIT or STRT.
1	R/W	STRT — Start
		Setting STRT clears the STOP bit (CSR0). STRT enables the LANCE to send and receive packets, perform direct memory access and do buffer management.
		STRT is read/write with 1 only. Writing a 0 into this bit has no effect.
		If STRT and INIT are set together, the INIT function will be executed first.
		STRT is cleared by bus RESET or setting the STOP bit (CSR0).

Bit	R/W	Description
0	R/W	INIT — Initialize 0 = No effect 1 = Starts LANCE initialization and reads the initialization block. Setting INIT clears the STOP bit (CSR0). If STRT and INIT are set together, the INIT function will be executed first. INIT is cleared by bus RESET or setting the STOP bit (CSR0).

Control and Status Register 1 (RAP = 1)

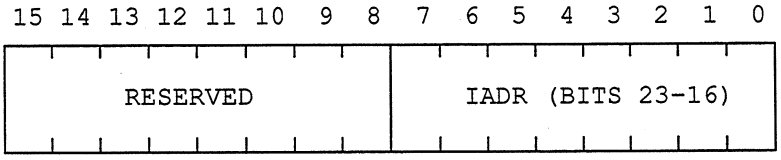


Bit	R/W	Description
15-1	R/W	IADR The low-order 16 bits of the address of the first word (lowest address) in the initialization block.
0	R/W	Always 0

CSR1 is accessible only when the STOP bit (CSR0) equals 1. If STOP equals 0, an access returns READY, a read operation returns undefined data and a write operation is ignored.

CSR1 is unaffected by bus RESET L.

Control and Status Register 2 (RAP = 2)

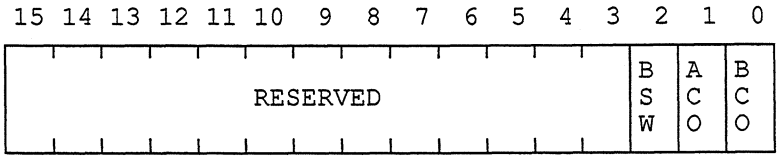


Bit	R/W	Description
15-8	R/W	RESERVED (Always 0)
7-0	R/W	IADR (Bits 23-16) The high order 8 bits of the address of the first word of the initialization block.

Accessible only when STOP equals 1 (CSR0). If STOP equals 0, an access returns READY, a read operation returns undefined data and a write operation is ignored.

CSR2 is unaffected by bus RESET L.

Control and Status Register 3 (RAP = 3)



Bit	R/W	Description
15-3	R/W	RESERVED (Always 0)
2	R/W	BSW — Byte swap 0 = The LANCE does not swap high and low bytes 1 = The LANCE swaps the high and low bytes on DMA data transfers between the silo and bus memory. BSW allows the LANCE to operate in systems that consider bits 15-8 to be the least significant byte and bits 7-0 to be the most significant byte. Only data from silo transfers is swapped; the initialization block data and the ring descriptor entries are NOT swapped. BSW is cleared by bus RESET or setting the STOP bit (CSR0).
1	R/W	ACO — Address latch enable (ALE) control 0 = ALE is asserted high. 1 = ALE is asserted low. ACO defines the assertive state of ALE when the LANCE is a bus master. ACO is cleared by bus RESET or setting the STOP bit (CSR0).
0	R/W	BCO — Byte mask control

BCO	I/O Pin 16	I/O Pin 15	I/O Pin 17
0	BM 1 L	BM 0 L	HOLD L
1	BUSAKO L	BYTE H	BUSRQ L

BCO redefines the byte mask and hold I/O pins.

BCO is cleared by bus RESET or setting the STOP bit (CSR0).

Table 2–2 lists the required values for each function of CSR3.

Table 2–2 LANCE CSR3 Required Values for the DEPCA

Bit	Function	Required Value
15-3	Undefined	Should be zero
2	BSW (Byte swap)	0
1	ACO (ALE control)	1
0	BCO (Byte mask control)	0

CSR3, which allows redefinition of the bus master interface, contains three bits. They are used to customize certain hardware interface signals provided by the LANCE when it is in bus master mode. The programming of these bits is hardware implementation dependent. The required values for the DEPCA are listed in Table 2–2.

CSR3 is accessible only when the STOP bit (CSR0) equals 1. If STOP equals 0, an access returns READY, a read operation returns undefined data and a write operation is ignored.

Bus RESET L or setting the STOP bit (CSR0), clears CSR3.

Initialization Block

During initialization, the LANCE reads operating parameters from the initialization block. Table 2–3 list the fields in the initialization block.

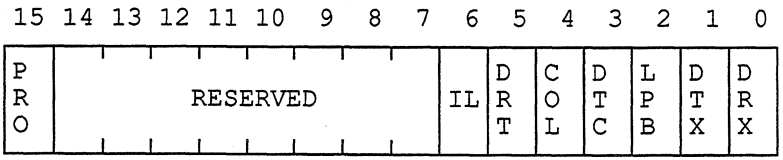
When INIT (CSR0) is set, the LANCE begins reading the initialization block. To ensure proper parameter initialization and LANCE operation, the controlling program should set INIT (CSR0) and then set STRT (CSR0). After the LANCE reads the initialization block, the LANCE sets IDON (CSR0). If INEA equals 1, the LANCE also generates an interrupt.

Table 2–3 Initialization Block

Field	Field Bits	Offset From IADR	Comment
TLEN-TDRA	23-16	+22	Higher addresses
TDRA	15-00	20	
RLEN-RDRA	23-16	+18	
RDRA	15-00	+16	
LADRF	63-48	+14	
LADRF	47-32	+12	
LADRF	31-16	+10	
LADRF	15-00	+08	
PADR	47-32	+06	
PADR	31-16	+04	
PADR	15-00	+02	
MODE	15-00	+00	Base address of block

The base address, IADR, is formed from CSR2 bits 7-0 and CSR1 bits 15-1.

Mode Field (Initialization Block, Offset 00H)



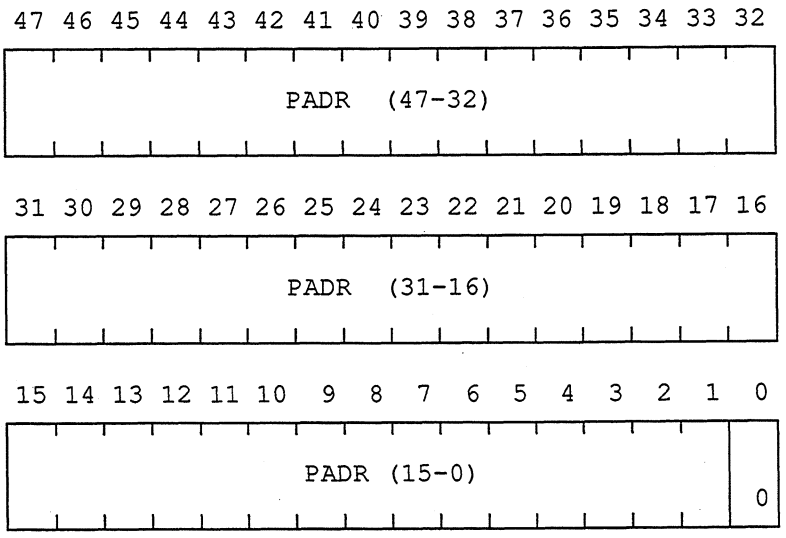
Bit	Description
15	PRO — Promiscuous 0 = Only incoming packets matching physical or logical address filter are accepted. 1 = All incoming packets are accepted.
14-7	RES — Reserved
6	IL — Internal loopback 0 = When LPB equals 1, specifies external loopback. 1 = When LPB equals 1, specifies internal loopback. IL is used with the LPB (bit 2) to determine where the loopback is to be done. Internal loopback allows the LANCE to receive its own transmitted packet. The maximum transmit packet size allowed during loopback is 32 data bytes. The LANCE automatically adds 4 bytes of CRC to the packet if DTC equals 0 and therefore the receive packet could be 36 bytes. IL is only valid if LPB = 1; otherwise it is ignored.
5	DRT — Disable retry 0 = LANCE attempts 15 retransmissions of a packet after the first collision before reporting a Retry error. 1 = LANCE attempts only one transmission of a packet. If there is a collision on the first transmission attempt, a Retry Error (RTY) is reported in Transmit Message Descriptor 3 (TMD3).
4	COL — Force collision 0 = Collision not forced 1 = Collision forced during subsequent transmission attempt COL allows the collision logic to be tested. For COL to be valid, the lance must be in internal loopback mode. When COL equals 1, 16 transmissions are attempted, and a retry error is reported in TMD3.

Bit	Description
3	DTC — Disable transmit CRC 0 = The transmitter generates and appends a CRC to the transmitted packet. 1 = The CRC logic is allocated to the receiver and no CRC is generated and sent with the transmitted packet. If DTC equals 0 during loopback, the CRC logic generates a CRC for the transmitted packet. CRC logic, shared by the receiver and the transmitter, cannot generate and check CRC at the same time. Therefore, the receiver does not check the CRC. The received data and CRC are written into memory and can be checked by the software. If DTC equals 1 during loopback, the software must append a CRC value to the transmit data in the transmit buffer. The receiver checks the CRC on the received data and reports any errors.
2	LPB — Loopback 0 = The LANCE operates in normal mode. 1 = For test purposes, the LANCE operates in full duplex loopback mode. The maximum transmit packet size is limited to 32 data bytes. If DTC equals 0, the LANCE automatically adds four CRC bytes. Thus, the received packet can be 36 bytes (32 bytes of data and 4 bytes of CRC). During loopback, the runt packet filter is disabled because the maximum packet is forced to be smaller than the minimum size Ethernet packet of 64 Bytes. Loopback mode allows simultaneous transmission and reception for a message constrained to fit within the silo. The LANCE waits until the entire message is in the silo before serial transmission begins. The incoming data stream fills the silo from behind as it is being emptied. Moving the received message out of the silo to memory does not begin until reception has ceased. In loopback mode, transmit data chaining is not possible. Receive data chaining is allowed, regardless of the receive buffer length. In normal operation, not loopback, the receive buffers must be at least 64 bytes long to allow time for buffer lookahead.
1	DTX — Disable the transmitter 0 = The LANCE can access the transmit descriptor ring. 1 = The LANCE can not access the transmit descriptor ring; therefore no transmissions are attempted. During initialization, if DTX equals 1, the TXON bit in CSR0 is cleared.

Bit	Description
0	DRX — Disable the receiver 0 = The LANCE receives incoming packets. 1 = The LANCE rejects incoming packets and does not access the receive descriptor ring. During initialization, if DRX equals 1, the RXON bit in CSR0 is cleared.

The mode field allows alteration of the LANCE operating parameters. In normal operation, the mode register is clear.

Physical Address Field (Initialization Block, Offset 02H)



The network physical address (PADR), is the unique 48-bit physical address assigned to the LANCE. PADR bit 0 must be zero.

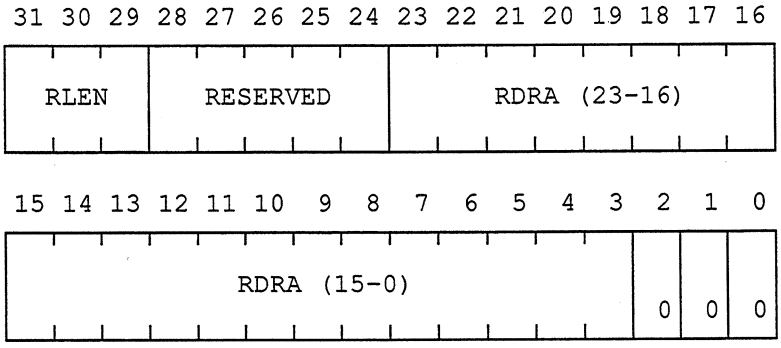
Logical Address Filter Field (Initialization Block, Offset 08H)

LADRF, the logical address filter field, is a 64-bit mask used by the LANCE to accept the logical addresses.

The logical address filter is a 64-bit mask that accepts incoming logical addresses sent through the CRC circuit. After all 48 bits of the address have travelled through the CRC circuit, the high-order 6 bits of the resultant CRC are strobed into a register. This register selects one of the 64-bit positions in the logical address filter. If the selected filter bit equals 1, the address is accepted and the packet is put in memory. The bit 0 of the incoming address must be 1 for a logical address. If bit 0 is 0, it is a physical address and is compared against the physical address that was loaded through the initialization block.

The broadcast address, which is all ones, does not go through the logical address Filter and is always enabled. If the logical address filter is loaded with all zeros, all incoming logical addresses except the broadcast address are rejected.

Receive Descriptor Ring Pointer Field (Initialization Block, Offset 10H)

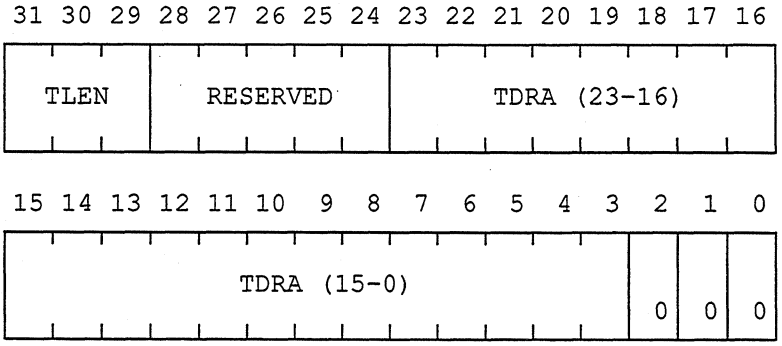


Bit	Description
31-29	RLEN — Receive ring length The number of entries in the receive ring expressed as a power of two.

RLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

28-24	RES — Reserved
24-0	RDRA — Receive descriptor ring address RDRA is the base address (lowest address) of the receive descriptor ring. Because the receive rings must be aligned on quadword boundaries, bits 2-0 must be zeros.

Transmit Descriptor Ring Pointer Field (Initialization Block, Offset 14H)



Bit	Description
31-29	TLEN — Transmit ring length The number of entries in the transmit ring expressed as a power of two.

TLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

28-24	RES — Reserved
24-0	TDRA — Transmit descriptor ring address TDRA is the base address (lowest address) of the transmit descriptor ring. Because the transmit rings must be aligned on quadword boundaries, bits 2-0 must be zeros.

Buffer Management

Buffer descriptors, organized as ring structures in memory, are used for buffer management. The buffer descriptors, also called message descriptors, are four words long and point to a buffer. Two ring structures are allocated for the LANCE: a ring of receive message descriptors (RMDs) and a ring of transmit message descriptors (TMDs). To transmit or receive packets, the LANCE polls each ring structure. The LANCE also enters status information in the descriptor entry. The LANCE is limited to looking only one descriptor entry ahead of the one with which the LANCE is currently working.

The location of the descriptor rings and their length are found in the initialization block, which the LANCE accesses during the initialization procedure. Writing a 1 into the STRT bit of CSR0 causes the LANCE to start accessing the descriptor rings and enables the sending and receiving of data packets.

The LANCE communicates with the data-link layer program through the ring structures in memory. Each entry in the ring is owned either by the LANCE or the data-link layer program. The ownership bit (OWN) in the message descriptor entry determines which owns the entry. Therefore, ownership of a descriptor entry is mutually exclusive. To gain ownership of a descriptor entry, the communications partner (LANCE or data-link layer program) must wait until the owner gives ownership to the communications partner. Between the time a communications partner relinquishes ownership of a descriptor entry and the time that communications partner regains ownership, it must not change any data in the descriptor entry.

Descriptor Rings in Memory

Figure 2–1 shows transmit descriptor rings with 128 message descriptors each. Figure 2–2 shows receive descriptor rings with 128 message descriptors each.

Figure 2–1 Transmit Descriptor Rings

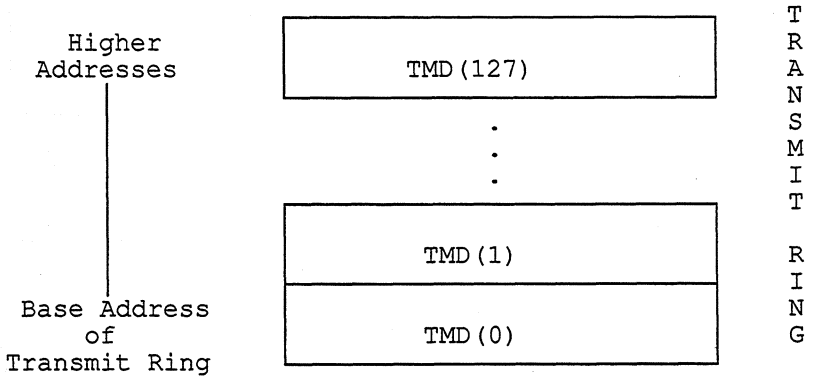
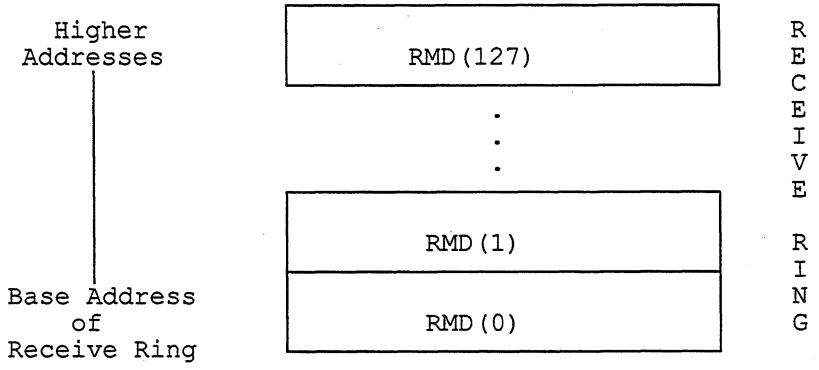


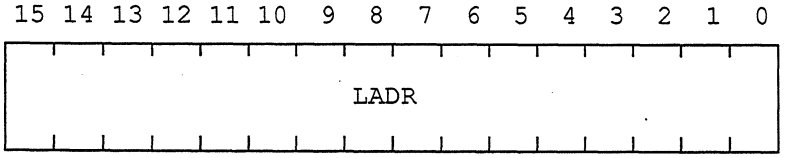
Figure 2–2 Receive Descriptor Rings



Receive Descriptor Rings

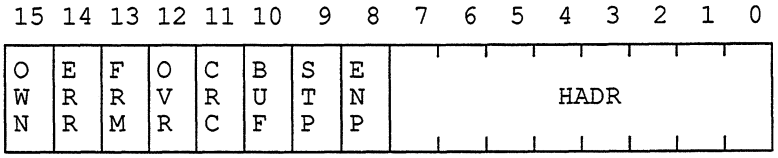
Each descriptor ring is a four-word entry (RMD0 through RMD3). The format of the receive descriptor entries follow.

Receive Message Descriptor 0 (RMD0)



Bit	Description
15-0	LADR — Low order address bits LADR is the lower 16 bits of a 24-bit buffer pointer. HADR (RMD1 bits 7-0) and LADR form a 24-bit pointer to the memory location in which the next received message is placed. LADR is written by the application software and remains unchanged by the LANCE.

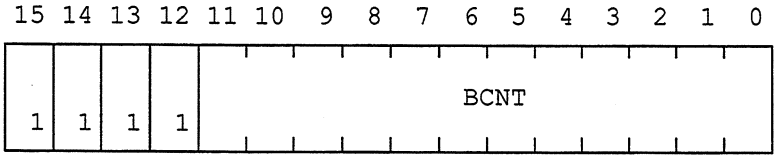
Receive Message Descriptor 1 (RMD1)



Bit	Description
15	OWN — RMD owner 0 = The descriptor entry is owned by the application software. 1 = The descriptor entry is owned by the LANCE. The LANCE clears the OWN bit after filling the buffer pointed to by the descriptor entry. The application software sets the OWN bit after emptying the buffer. Once the LANCE or application software has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	ERR — Error 0 = The four bits, FRM, OVR, CRC, and BUF, are all equal to zero. 1 = One or more of the four bits, FRM, OVR, CRC, or BUF, is equal to one. ERR is set by the LANCE and cleared by the application software.
13	FRM — Framing error 0 = No framing error 1 = The incoming packet contained a noninteger multiple of eight bits and there was a CRC error. A CRC error on the incoming packet is a necessary condition for FRM to equal 1 (even if there was a noninteger multiple of eight bits in the packet). FRM is set by the LANCE and cleared by the application software.
12	OVR — Overflow Error 0 = No overflow error 1 = Because the receiver could not store a packet in a memory buffer before the internal silo overflowed, the receiver has lost all or part of the incoming packet. OVR is set by the LANCE and cleared by the application software.

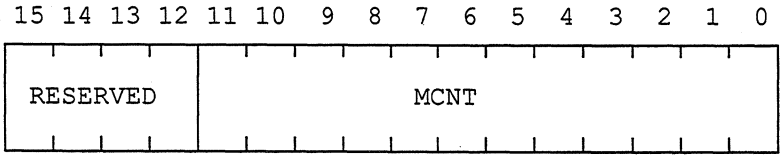
Bit	Description
11	CRC — Cyclic redundancy check 0 = No CRC error 1 = The receiver detected a CRC error on the incoming packet. CRC is set by the LANCE and cleared by the application software.
10	BUF — Buffer error 0 = No buffer error 1 = While data chaining a received packet, the LANCE did not own the next buffer. This condition occurs when the OWN bit of the next buffer is zero or the LANCE can not acquire the next status before silo overflow occurs. BUF is set by the LANCE and cleared by the application software.
9	STP — Start of packet 0 = This is not the first buffer the LANCE used for this packet. 1 = This is the first buffer the LANCE used for this packet. STP is used for data chaining buffers. STP is set by the LANCE and cleared by the application software.
8	ENP — End of packet 0 = This is not the last buffer used by the LANCE for this packet. 1 = This is the last buffer used by the LANCE for this packet. ENP is used for data-chaining buffers. When both STP and ENP are set, the packet fits into one buffer and there was no data chaining. ENP is set by the LANCE and cleared by the application software.
7-0	HADR — High order address bits HADR is the upper eight bits of a 24-bit buffer pointer. HADR and LADR (RMD0 bits 15-0) form a 24-bit pointer to the memory location in which the next received message is placed. This field is written by the application software and remains unchanged by the LANCE.

Receive Message Descriptor 2 (RMD2)



Bit	Description
15-12	Must be ones. These fields are written by the application software and remain unchanged by the LANCE.
11-0	BCNT — Buffer byte count BCNT is the length of the buffer pointed to by this descriptor expressed as a two's complement number. This field is written by the application software and remains unchanged by the LANCE. The minimum buffer size is 64 bytes.

Receive Message Descriptor 3 (RMD3)

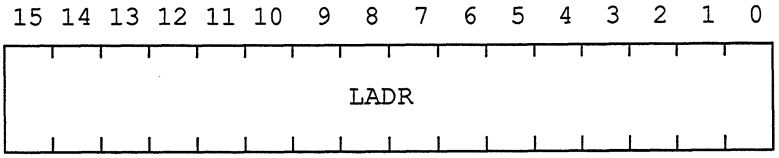


Bit	Description
15-12	Reserved and read as zeros.
11-0	MCNT — Message byte count MCNT is the length in bytes of the received message. MCNT is valid only when ERR is clear and ENP is set. MCNT is written by the LANCE and cleared by the application software. When data chaining, RMD3 is loaded by the LANCE only when the status of the last buffer is updated. Only the status word is updated for the other buffers in the data chain.

Transmit Descriptor Rings

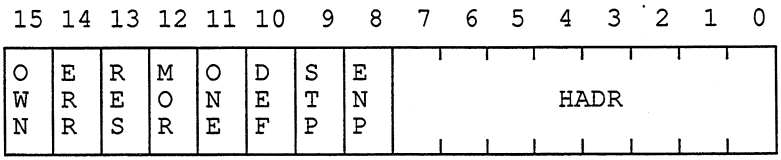
Each descriptor ring is a 4-word entry (TMD0 through TMD3). The format of the transmit descriptor entries follow.

Transmit Message Descriptor 0 (TMD0)



Bit	Description
15-0	LADR — Low order address bits LADR is the lower 16 bits of a 24-bit buffer pointer. HADR (TMD1 bits 7-0) and LADR form a 24-bit pointer to the memory location containing the next message to be transmitted. LADR is written by the application software and remains unchanged by the LANCE.

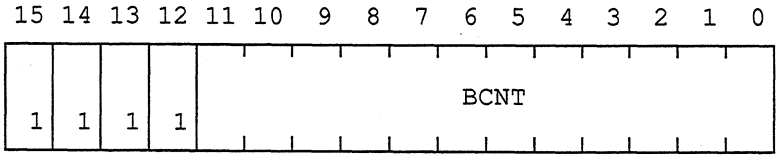
Transmit Message Descriptor 1 (TMD1)



Bit	Description
15	OWN — TMD owner 0 = The descriptor entry is owned by the application software. 1 = The descriptor entry is owned by the LANCE. The application software sets the OWN bit after filling the buffer. The LANCE clears the OWN bit after transmitting the buffer pointed to by the descriptor entry. Once the LANCE or application software has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	ERR — Error 0 = The four bits, LCO, LCA, UND, and RTY, are all equal to zero. 1 = One or more of the four bits, LCO, LCA, UND, or RTY, is equal to one. ERR is set by the LANCE and cleared by the application software.
13	RES — Reserved The LANCE writes a zero to this field.
12	MOR — More 0 = The packet was transmitted within one retry. 1 = More than one retry was required to transmit the packet.
11	ONE 0 = The packet was not transmitted with exactly one retry. 1 = The packet was transmitted with exactly one retry.

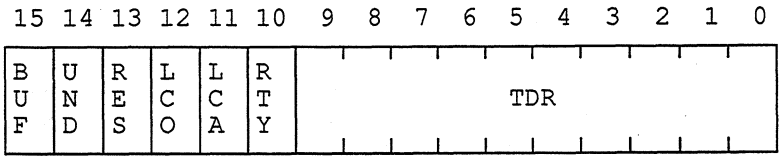
Bit	Description
10	DEF — Defer 0 = The LANCE did not have to defer before transmitting a packet. 1 = While trying to transmit a packet, the channel was busy and the LANCE had to defer. DEF is set by the LANCE and cleared by the application software.
9	STP — Start of packet 0 = This is not the first buffer the LANCE should use to transmit this packet. 1 = This is the first buffer the LANCE should use to transmit this packet. STP is used for data chaining buffers. STP is set by the application software and remains unchanged by the LANCE.
8	ENP — End of packet 0 = This is not the last buffer that the LANCE should use for this packet. 1 = This is the last buffer that the LANCE should use for this packet. ENP is used for data chaining buffers. When both STP and ENP are set, the packet fit into one buffer and there was no data chaining. ENP is set by the application software remains unchanged by the LANCE.
7-0	HADR — High order address bits HADR is the upper eight bits of a 24-bit buffer pointer. HADR and LADR (TMD0 bits 15-0) form a 24-bit pointer to the memory location containing the next message to be transmitted. This field is written by the application software and remains unchanged by the LANCE.

Transmit Message Descriptor 2 (TMD2)



Bit	Description
15-12	Must be ones. These fields are written by the application software and remains unchanged by the LANCE.
11-0	BCNT — Buffer byte count BCNT is the length of the buffer pointed to by this descriptor expressed as a two's complement number. This field is written by the application software and remains unchanged by the LANCE. The minimum buffer size is 64 bytes.

Transmit Message Descriptor 3 (TMD3)



Bit	Description
15	BUF — Buffer error 0 = No buffer error 1 = During a transmission, the LANCE did not find the ENP flag in the current buffer and the LANCE did not own the next buffer. If the LANCE owns the next buffer, but can not read the next buffer's status parameters before the silo underflows, BUF is also set. BUF is set by the LANCE and cleared by the application software. If a Buffer Error occurs, an Underflow Error also occurs because the transmitter continues to read data from the silo until it is empty.
14	UND — Underflow error 0 = No underflow error 1 = Because of a lack of data from memory, the transmitter truncated a message. UND indicates that the silo was emptied before the end of the packet was reached. When this condition occurs, the transmitter is disabled (TXON is cleared.) UND is set by the LANCE and cleared by the application software.
13	RES — Reserved (Always 0)
12	LCO — Late collision 0 = No collision 1 = A collision occurred after the slot time of the channel elapsed. The LANCE does not retry on late collisions. LCO is set by the LANCE and cleared by the application software.

Bit	Description
11	LCA — Loss of carrier 0 = The carrier input has not gone false during transmission. 1 = The carrier presence input to the LANCE went false during a transmission that was initiated by the LANCE. The LANCE does not retry upon loss of carrier. LCA is set by the LANCE and cleared by the application software.
10	RTY — Retry error 0 = No retry error 1 = In 16 attempts, the transmitter has failed to transmit a message due to repeated collisions on the medium. If the mode field DRT equals 1, RTY sets after 1 failed transmission attempt. RTY is set by the LANCE and cleared by the application software.
9-0	TDR — Time domain reflectometry TDR shows the state of an internal LANCE counter that counts from the start of a transmission to the occurrence of a collision. This value is useful in determining the approximate distance to a cable fault. The TDR value is written by the LANCE and is valid only if RTY is set.

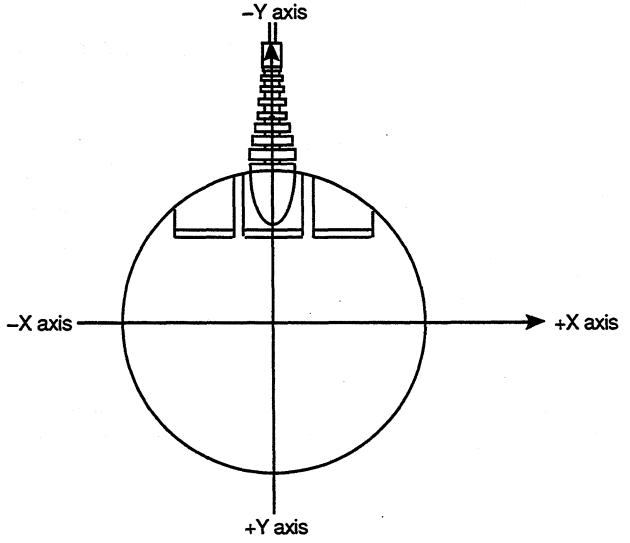
TMD3 is valid only if the LANCE has already set the ERR bit of TMD1.

3
Mouse Information

Introduction

The DIGITAL mouse is a pointing device with three input switches. The mouse has two encoders, one for the X axis and one for the Y axis. The encoders have a resolution of 200 counts per inch. When moved on a flat surface, the mouse monitors the motion relative to its position at the beginning of the motion. Thus, the mouse maintains positional data in the form of incremental X/Y encoder counts. Figure 3–1 shows the mouse in relation to its X/Y axes.

Figure 3–1 DIGITAL Mouse



Communication Requirements

The mouse communicates through an asynchronous serial interface at 4800 baud. Data bytes have the following format:

- 1 start bit
- 8 data bits (least significant bit first)
- 1 parity bit (the mouse transmits odd parity, but ignores receive parity errors.)
- 1 stop bit

If a byte is sent to the mouse while the mouse is transmitting, the mouse aborts the transmission and processes the new command. If the mouse receives a byte between the characters of a multibyte report, the mouse is considered to be transmitting and aborts the report.

The workstation communicates with the mouse through an asynchronous serial interface (Signetics SCN2661 Enhanced Programmable Communications Interface).

The Signetics' document, *Microprocessor Data Manual 1986*, provides additional information on the SCN2661.

Mouse Commands

Table 3–1 lists the mouse commands. The commands are issued by transmitting the appropriate command code.

Table 3–1 Mouse Command Summary

ASCII Value	Hex Value	Function
D	44H	Prompt Mode
R	52H	Incremental Stream Mode
P	50H	Request Mouse Position
T	54H	Invoke Self-test
Zx	5AH xx	Vendor Reserved function

Modes

The mouse has two operating modes, prompt mode and incremental stream mode. In prompt mode, which is the powerup default, the mouse generates a report in response to a request mouse position command. In incremental stream mode, whenever the mouse moves it generates a report of that movement. It also reports a change in button position since the last report. No report is generated when the mouse is motionless and no buttons have been changed.

Request Mouse Position

The mouse responds to this command by sending a position report and switching to prompt mode.

Invoke Self-Test

The mouse responds to this command by executing a self-test and then sending a self-test report. Self-test leaves the mouse in the reset or powerup state. During the self-test, any data sent to the mouse is ignored until the last byte of the self-test report has been sent by the mouse. The 4-byte self-test report consists of a 2-byte identification code and a 2-byte status code.

Vendor Reserved Function

The vendor reserved function is a 2-byte command, the ASCII character "Z" followed by any printable character. This command allows vendors to add special mouse functions. Normally, these functions are for quality control. The manufacturer determines these functions, which may include transmitting specialized reports. These commands may not include new modes. On completion of a vendor reserved function, the mouse must be restored to its previous state.

Mouse Reports

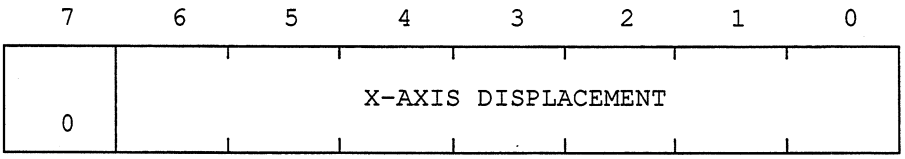
The mouse can transmit two reports, a 3-byte position report and a 4-byte self-test report.

Position Report — Byte 1

7	6	5	4	3	2	1	0
1	0	0	SIGN-X	SIGN-Y	LEFT BUTTON	MIDDLE BUTTON	RIGHT BUTTON

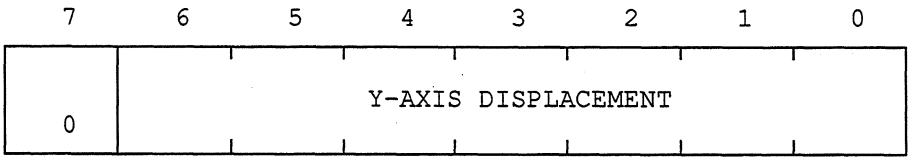
Bit	Description
7	Always 1
6-5	Always 0
4	SIGN-X (Sign bit for X-axis displacement) 0 = Negative X-axis displacement 1 = Positive X-axis displacement
3	SIGN-Y (Sign bit for Y-axis displacement) 0 = Negative X-axis displacement 1 = Positive X-axis displacement
2	LEFT BUTTON 0 = Switch open 1 = Switch closed
1	MIDDLE BUTTON 0 = Switch open 1 = Switch closed
0	RIGHT BUTTON 0 = Switch open 1 = Switch closed

Position Report — Byte 2



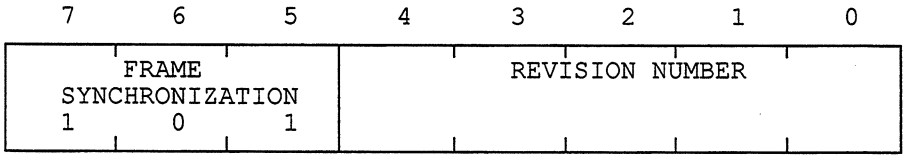
Bit	Description
7	Always 0
6-0	X-AXIS DISPLACEMENT The X-axis displacement is measured in encoder counts (200 per inch). The value returned in this byte is the distance moved since the last report. In prompt mode, if reports are not requested often enough, this value can overflow. If an overflow occurs, no indication is given. Bit 0 is the least significant bit.

Position Report — Byte 3



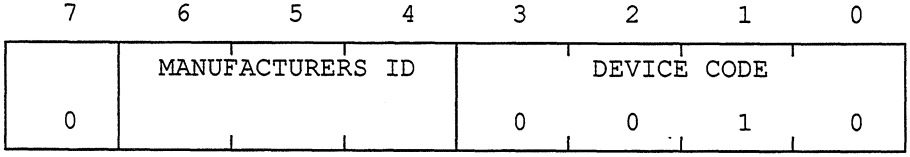
Bit	Description
7	Always 0
6-0	Y-AXIS DISPLACEMENT The Y-axis displacement is measured in encoder counts (200 per inch). The value returned in this byte is the distance moved since the last report. In prompt mode, if reports are not requested often enough, this value can overflow. If an overflow occurs, no indication is given. Bit 0 is the least significant bit.

Self-Test Report — Byte 1



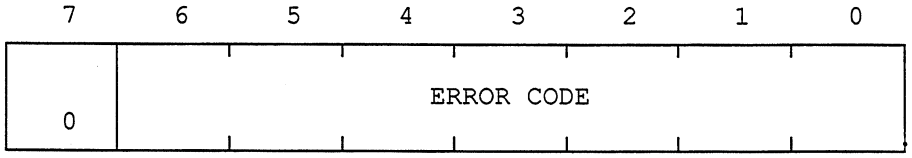
Bit	Description
7-5	FRAME SYNCHRONIZATION These bits are always 101. They provide a means of detecting the first byte of a self-test report.
4-0	REVISION NUMBER This is a hardware and software revision number for this design cycle.

Self-Test Report — Byte 2



Bit	Description
7	Always 0
6-4	MANUFACTURERS ID
3-0	DEVICE CODE
	Always 0010

Self-Test Report — Byte 3



Bit	Description
7	Always 0
6-0	ERROR CODE 00H = No error 3EH = RAM or ROM checksum error 3DH = Button error

Self-Test Report — Byte 4

7	6	5	4	3	2	1	0
0	0	0	0	0	LEFT BUTTON	MIDDLE BUTTON	RIGHT BUTTON

Bit	Description
7-3	Always 0
2	LEFT BUTTON 0 = Switch good 1 = Switch closed or failed
1	MIDDLE BUTTON 0 = Switch good 1 = Switch closed or failed
0	RIGHT BUTTON 0 = Switch good 1 = Switch closed or failed

Serial Interface

The serial interface is a SIGNETICS SCN2661 Enhanced Programmable Communications Interface. Table 3–2 lists the input/output (I/O) ports that access the serial interface registers.

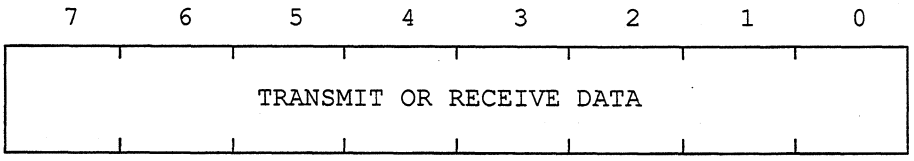
Table 3–2 Serial Interface Registers

Primary Address	Secondary Address	R/W	Register Name
0308H	0208H	R	Receive buffer
		W	Transmit holding register
0308H	0208H	R	Status register
		W	Syn1/Syn2/DLE registers †
030AH	020AH	R/W	Mode register 1 and mode register 2 ‡
030BH	020BH	R/W	Command register

†The Syn1, Syn2, and DLE registers are not used.

‡Mode registers 1 and 2 are accessed at the same I/O address. To read either mode register 1 or 2, read mode register 1 first and then read mode register 2. To write either mode register 1 or 2, write mode register 1 first and then write mode register 2. Mode register 1 must be accessed to access mode register 2.

Transmit Holding Register and Receive Buffer



Bit	Description	
7-0	R	Accesses the receive data buffer
	W	Accesses the transmit holding register

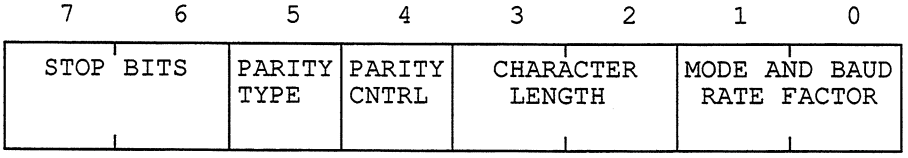
Status Register

7	6	5	4	3	2	1	0
DATA SET READY 1	DATA CAR. DETECT 1	FRAME ERROR	OVER RUN	PARITY ERROR	DATA SET READY CHANGE	RxRDY	TxRDY

Bit	Description	
7	R	DATA SET READY (always 1)
6	R	DATA CARRIER DETECT (always 1)
5	R	FRAMING ERROR 0 = Normal 1 = Framing error This bit is cleared by disabling the receiver, issuing the reset error command, or reading the status register.
4	R	OVERRUN 0 = Normal 1 = Overrun error This bit is cleared by disabling the receiver or issuing the reset error command.
3	R	PARITY ERROR 0 = Normal 1 = Parity error (if parity checking is enabled) This bit is cleared by disabling the receiver, issuing the reset error command, or receiving another character.
2	R	DATA SET READY CHANGED (always 0)
1	R	RxRDY — Receive Data Ready 0 = Receive buffer is empty 1 = Receive buffer contains data and an interrupt is pending This bit is cleared by reading the receive buffer or disabling the receiver (command register bit 2).

Bit		Description
0	R	TxRDY — Transmit Holding Register Ready 0 = Transmit holding register busy 1 = Transmit holding register empty and an interrupt is pending This bit is cleared by writing the transmit holding register or disabling the transmitter (command register bit 0).

Mode Register 1

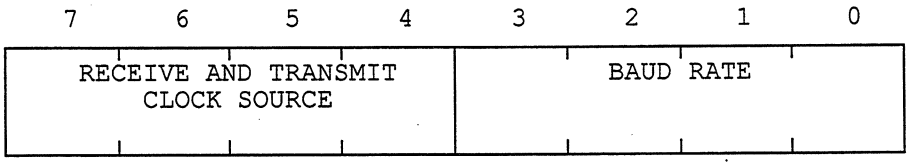


Bit	R/W	Description
7-6	R/W	STOP BITS 00 = Invalid 01 = 1 stop bit 10 = 1-1/2 stop bits 11 = 2 stop bits
5	R/W	PARITY TYPE 0 = Odd parity 1 = Even parity
4	R/W	PARITY CONTROL 0 = Parity checking disabled 1 = Parity checking enabled
3-2	R/W	CHARACTER LENGTH 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits
1-0	R/W	MODE AND BAUD RATE FACTOR 00 = Synchronous 1 X rate 01 = Asynchronous 1 X rate 10 = Asynchronous 16 X rate 11 = Asynchronous 64 X rate

Mode registers 1 and 2 are accessed at the same I/O address. To read either mode register 1 or 2, read mode register 1 first and then read mode register 2. To write either mode register 1 or 2, write mode register 1 first and then write mode register 2. Mode register 1 must be accessed to access mode register 2.

When programming mode register 1, use a value of 5EH.

Mode Register 2



Bit	Description
7-4	RECEIVE AND TRANSMIT CLOCK SOURCE For the DEPCA hardware, this value is fixed.
3-0	BAUD RATE See Table 3–3.

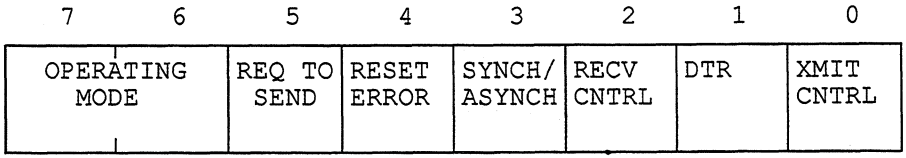
Mode registers 1 and 2 are accessed at the same I/O address. Read mode register 1 and then read mode register 2, or write mode register 1 and then write mode register 2. Mode register 1 must be accessed to access mode register 2.

When programming mode register 2, use a value of 7CH.

Table 3–3 Baud Rate Table

Bits 3-0	Baud Rate	Bits 3-0	Baud Rate
0000	50	1000	1800
0001	75	1001	2000
0010	110	1010	2400
0011	134.5	1011	3600
0100	150	1100	4800
0101	300	1101	7200
0110	600	1110	9600
0111	1200	1111	19200

Command Register



Bit	R/W	Description
7-6	R/W	OPERATING MODE 00 = Normal operation 01 = Asynchronous (automatic echo mode) 10 = Local loop back 11 = Remote loop back
5	R/W	REQUEST TO SEND 0 = Force request to send output high (disables interrupt buffer) 1 = Force request to send output low (enables interrupt buffer) The 2661 EPCI has a buffer between the interrupt output line and the peripheral interrupt controller input. This buffer is controlled by bit 3. Enabling the buffer enables the 2661 EPCI interrupt output line.
4		RESET ERROR
	R	Always 0
	W	0 = No effect 1 = Reset error flags (parity, framing, overrun)
3	R/W	SYNCH/ASYNCH 0 = Normal 1 = Force break
2	R/W	RECEIVE CONTROL 0 = Disable receiver, receive interrupt, and status register bit 1 1 = Enable receiver, receive interrupt, and status register bit 1
1	R/W	DTR — Data Terminal Ready (output not connected) 0 = Force data terminal ready output high 1 = Force data terminal ready output low

Bit	R/W	Description
0	R/W	XMIT CONTROL — Transmit Control 0 = Disable transmitter, transmit interrupt, and status register bit 0 1 = Enable transmitter, transmit interrupt, and status register bit 0

When programming the command register, use a base value of 30H. In addition to the base value, bits 0 and 3 (transmit and receive control) must be applied as required.

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